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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : G11C 7/00, 11/40

A1

(11) International Publication Number: **WO 00/08649**

(43) International Publication Date: 17 February 2000 (17.02.00)

(21) International Application Number: PCT/KR99/00086

(22) International Filing Date: 26 February 1999 (26.02.99)

(30) Priority Data:
1998/32022 6 August 1998 (06.08.98) KR

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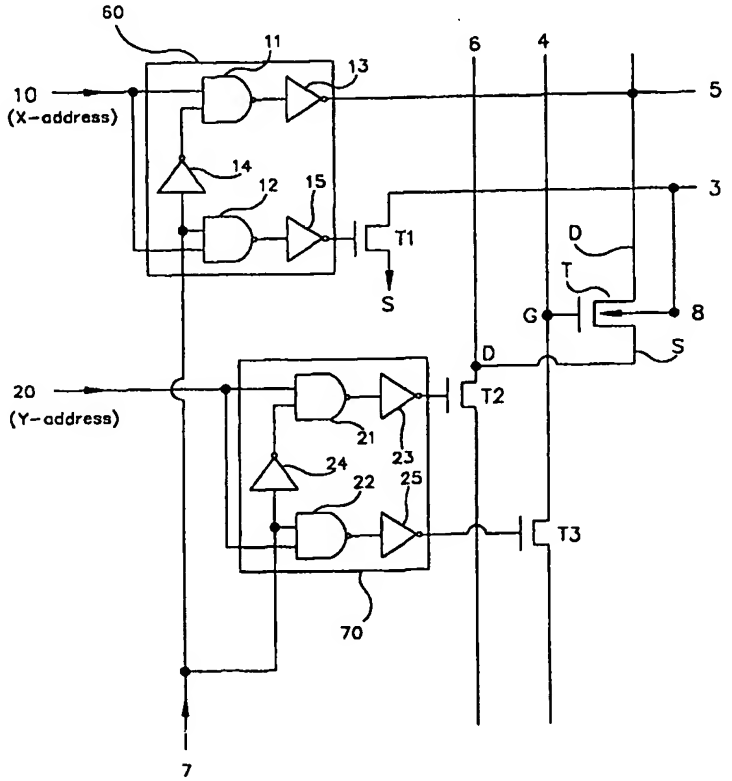
(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published
With international search report.

(54) Title: MEMORY DEVICE USING A TRANSISTOR AND ITS FABRICATION METHOD

(57) Abstract

The present invention provides a memory device by using a single transistor, comprising a circuit including a gate of a memory cell and a P type well substrate for inputting(writing) information and another circuit including a source and a drain for outputting(reading) information. In other word, the memory device includes an information input/output circuit by using a pair of respective read and write terminals. The transistor comprises a source, a drain, and a ferroelectric element gate which are formed in a P type (or N type) well substrate. And the present invention provides a fabrication method for manufacturing the memory circuit, comprising depositing the P type (or N type) well structure on a Si wafer and forming the source, the drain and then the gate in the P type (or N type) well structure.



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Memory device using a transistor and its fabrication method

TECHNICAL FIELD

The present invention relates generally to a memory device using a single transistor and its fabrication method, in which the transistor comprises a source(S), a drain(D), and a ferroelectric gate(G) which are formed in a P type(or N type) well substrate for reading/writing data. The P type(or N type) well substrate is formed by diffusing doping sources. More particularly, the present invention relates to a non-volatile, non-destructive read-out memory device, which may read out a stored data without destroying the data, and its fabrication method.

BACKGROUND ART

The subject matter of the present application is disclosed in U.S. Patent No. 5559733, filed June 7, 1995 and U.S. Patent No. 5686745, filed June 19, 1995.

In general, a semiconductor memory is called a dynamic RAM(DRAM). The DRAM is a device capable of storing/choosing for reading the data by using a memory cell. Here, the memory cell comprises a transistor and a capacitor. Additionally, the DRAM performs a large capacity of memory function as integrating the memory cells. An integration rate of the memory cell now becomes higher and higher continuously according to technology of a very large scale integration(VLSI).

The DRAM always leads a most advanced microelectronic technology symbolized by device miniaturizing process, subminiature device and circuit design technology. The DRAM is a device of a mass product because a general manufacturing process is stabilized and a circuit design is rarely changed. Advance of the device miniaturization shows an increment of the DRAM integration rate. Since 1Kbyte DRAM showed in the 1970s, the capacity of the DRAM is increased almost 4 times of it at every 3 years and finally, the prototype of 1Giga DRAM was realized in 1998.

The high integration and large capacity of the DRAM are established by a bipolar transistor technology in the 1960s, in which the bipolar transistor may be operated with a high-speed even though it requires a large usage power. But an MOS technology is practically used because the manufacturing process is simple and requires low power dissipation since 1970s, and a CMOS technology having better low power dissipation, is now applied to the DRAM.

FIG. 1 is a circuitry diagram of a memory cell of a DRAM.

Referring to FIG. 1, the DRAM comprises a transistor as a switch, and a

capacitor for storing data. A word line 1 is selected by an X-Address and a bit line 2 is selected by a Y-Address on a semiconductor memory which is fabricated by integrating the memory cells. Thereby, a cell data of the selected location is amplified and read externally. Binary "0" and "1" states, which are switched by applying a voltage pulse of sufficient magnitude. Here, binary information, "1" or "0" is corresponded to whether the capacitor of the memory cell has a charge or not, in other words, a terminal voltage of the cell capacitor is higher or lower than a predetermined value.

When the voltage in accordance with the binary information is applied to the memory cell, "write" process is performed. And what the capacitor has the charge or not causes the voltage change to higher or lower, thereby "read" process is performed as a detecting it to an external memory cell. Data maintenance has ideally no power usage because the capacitor accumulates the charges.

But, there is a leak current in a PN junction of the MOS transistor, and the stored initial charge is therefore reduced. As a result, the data is lost. Accordingly, before losing the data, the capacitor should be recharged as much as the initial charge by matching the read information after reading the data of the memory cell. The memory maintains the data by which the above procedures should be repeated periodically. The recharging process is called refresh operation. The DRAM(Dynamic-RAM) is called because the data maintenance is dynamically accomplished through the repetition of the refresh operation.

In addition to the DRAM, there are a static RAM(SRAM), a ferroelectric RAM(FRAM), etc. The SRAM is used in a main memory of a supercomputer or a cache memory of a common calculator or a cache memory having a microprocessor because of having durability of the information storage. And also it is commonly used for portable devices because the SRAM requires a low usage power for storing the data, even though there are disadvantages that manufacturing procedure is more complicated and it is more expensive than the DRAM to manufacture.

The FRAM is a new memory device which may successively store the data as using a memory cell, similar to DRAM, without supplying a power source. There are two kinds of FRAM ; a destructive and a non-destructive type. The destructive FRAM comprises a transistor as a switch for reading/writing information and a capacitor of storing data. The destructive FRAM is similar to the DRAM except that the destructive FRAM uses a ferroelectric material as a capacitor. The ferroelectric material generates a spontaneous polarization without power source, it is therefore possible to have a continuous storage ability because of maintaining an electric characteristic

successively. However, it should be required to reset that the information should be rewritten when the information stored in the capacitor is destroyed.

The non-destructive FRAM may perform a switching function with a single transistor as well as an information storage function, as an absolutely new memory device.

Accordingly, the non-destructive FRAM having a very simple structure, may improve an integration rate 10 times, comparing with the conventional DRAM or the destructive FRAM which have a single transistor and a single capacitor. The non-destructive FRAM including advantages of the DRAM and the destructive FRAM, may successively store information without power source, may use for a long time because of not requiring the reset function, and helps to establish a simple circuit.

DISCLOSURE OF INVENTION

However, it has not been invented the device structure, its fabrication method, and the subsidiary circuit of the non-destructive FRAM consisting of a single transistor for reading/writing information.

This invention is to resolve the problems described earlier and an object of the present invention is to provide the memory device structure, the fabrication method, and the subsidiary circuit of the non-destructive FRAM consisting of a single transistor for reading/writing information. The single transistor consists of a source, a drain, a ferroelectric gate, and a P type (or N type) well substrate. The ferroelectric gate and P type (or N type) well substrate are using for inputting(writing) information and a source and a drain are using for outputting(reading) information. Therefore, the memory device has four terminals. In other words, the subsidiary circuit uses the four terminals for writing and reading information; two terminals (a gate and a substrate) for writing and two terminals (a source and a drain) for reading.

BRIEF DESCRIPTION OF DRAWINGS

FIG. 1 is a circuitry diagram of a unit memory cell of a DRAM,

FIG. 2 is a circuitry diagram of a unit memory cell of a memory device consisting of a single transistor in accordance with the present invention,

FIG. 3 is a circuitry diagram for inputting and outputting data to the unit memory cell of the FIG. 2,

FIG. 4 shows a mask pattern for fabricating the unit memory cell of the memory device comprised a single transistor,

FIG. 5 is a schematic cross sectional view showing the unit memory cell of the memory device comprised a single transistor, and

FIG. 6 is a flowchart explaining a fabrication procedure of the unit memory cell of the memory device comprised the single transistor.

BEST MODE FOR CARRYING OUT THE INVENTION

Embodiments of the invention will be described with reference to the accompanying drawings.

FIG. 2 is a circuitry diagram of a unit memory cell of a memory device consisting of a single transistor in accordance with the present invention.

FIG. 3 is a circuitry diagram for inputting and outputting data to the unit memory cell of the FIG. 2.

First, let's explain the circuitry diagram of the unit memory cell referring to FIG. 2. The unit memory cell has four terminals; a source, a drain, a ferroelectric gate, and a P type (or N type) well substrate. For writing data, a gate (G) terminal which is connected to a Write Bit Line (4) for writing and a P type(or N type) well substrate which is connected to a Write Word Line (8) for writing are used. And for reading the data, a source(S) terminal which is connected to a Read Word Line (5) for reading and a drain(D) terminal which is connected to a Read Bit Line (6) for reading are used. Therefore, terminals for writing data which consist of Write Bit Line (4) and Write Word Line (8) are electrically separated from terminals for reading data which consist of Read Word Line (5) and Read Bit Line (6).

Second, the input/output circuit for writing/reading the data on the unit memory cell of the memory device is explained. Here the memory device uses a single transistor as shown in FIG. 3.

The input/output circuit in FIG. 3 comprises a transistor (T) which stores and outputs the data. Logic Circuit 1 (60) which consists of two NAND gate(11 and 12) and three inverters (13, 14 and 15), and Logic Circuit 2(70) which consists of two NAND gates (21 and 22) and three inverters (23, 24 and 25). And the input/output circuit further comprises three transistors (T1, T2 and T3) for connecting the Logic Circuit 1 (60) and Logic Circuit 2 (70) to the transistor (T) in order to store/output the data to the transistor (T). And also the input/output circuit comprises a Write Bit Line (4) for writing and a Write Word Line (3) for writing which are data writing terminals, a Read Word Line (5) for reading and a Read Bit Line (6) which are data reading terminals. Finally, the input/output circuit further comprises Word Line 1 (10) of inputting an X-

address signal and Word Line 2 (20) of inputting a Y-address signal.

Referring to FIG. 3, the operation principles of the invention are going to be described.

First, it is described how to input the data.

When a writing X-address signal through Word Line 1 (10) and a write enable signal (7) are inputted to the NAND gate (11 and 12) of the Logic Circuit 1 (60), the transistor 1 (T1) connected to Logic Circuit 1(60) turns "on". Because the P type (or N type) well substrate (8) of the transistor (T) is grounded through the grounded source (S) of the transistor 1 (T1), thereby the transistor (T) is selected among the unit devices. In order to input a data "1" to the transistor (T), voltage of +Vcc is applied to the gate (G) of the transistor (T) through the Write Bit Line (4) for writing.

During writing "1" to the transistor (T), the source (S) should be floating, whereas it does not matter which data is inputted to the drain (D). In other words, when the Y-address signal through Word Line 2 (20) and a write enable bar signal are inputted to the NAND gate (21 and 22) of Logic Circuit 2 (70) connected to the transistor 2 (T2), "0" signal is applied to the gate (G) of the transistor 2 (T2) connected to an output terminal of the Logic Circuit 2 (70). Therefore, the transistor 2 (T2) turns "off" and the source (S) of the transistor (T) is therefore floating. Here the "floating" state means that no voltage is applied and no ground is connected to the terminal. In addition, because an X-address signal and a write enable bar signal are inputted to the drain (D) of the transistor (T), it is grounded by "0" signal. Accordingly, the transistor (T), which is selected among the unit devices by the P type (or N type) well substrate, can be input the data "0" or "1". The gate (G) of the transistor (T) is comprised of metal, ferroelectric material, insulator and silicon.

Now it is described how to store (write) the data by applied voltage to the gate (G) of the transistor (T).

In contrast to the capacitor of DRAM in which stores information by a stored charge, the present invention uses a bistable nonvolatile polarization state based on a ferroelectric effect. Ferroelectric materials, such as $SrBi_2Ta_2O_9$(SBT), $PbZrTiO_3$(PZT), PbLnZrTiO3(PLZT), $BaSrTiO_3$(BST), and $SrBi_2TNb_2O_9$(SBTN) polarize spontaneously under the influence of an external field and to remain polarized even after the external field is removed. In other words, when voltage +Vcc is applied to the gate (G), the ferroelectric material polarizes downward and stores the data of "1". Then, the information of data of "1" remains even after the voltage +Vcc applied to the gate (G) is removed. Meanwhile, the polarization can be reversed by applying a field

of opposite polarity. In other words, when voltage –Vcc is applied to the gate (G), the ferroelectric material polarizes upward and stores the data of "0". Then, the information of data of "0" remains even after the voltage –Vcc applied to the gate (G) is removed. Here, for the convenience, we name the applied voltage of +Vcc or –Vcc to write the data the "write voltage". On the other hand, when the voltage is used for reading the data, we name it "read voltage".

The data of "0" or "1" can be stored in the particular transistor(T) by designating an address assigned by a row and a column of the unit device by the signal inputted through the circuit of the Write Word Line (3) for writing and the Write Bit Line (4) for writing.

Next it is described how to output (read) the data.

The data can be read by sensing the interaction of a read field with the polarization state of the ferroelectric material. If a "read voltage" is applied to the ferroelectroc material of polarity opposite to the previous "write voltage", the polarization state will switch, giving rise to a large displacement charge that can be sensed by proper circuitry. In other words, in order to read the stored data in the transistor (T), a writing X-address signal through Word Line 1(10) and a write enable bar signal through Word Line(5) for reading are inputted to the NAND gates (11 and 12) of the Logic Circuit 1(60), then the voltage +Vcc is applied to the drain (D) of the transistor (T). In addition, the Y-address signal and a write enable bar signal through Word Line 7 are inputted to the NAND gates (21 and 22) of the Logic Circuit 2(70) and the voltage +Vcc is applied to a gate of the transistor 2 (T2). Thereby, the transistor 2 (T2) turns "on" and selection is finally completed to read the data stored in the transistor (T).

After completed the selection, the data is transmitted to a supervising circuit through the Read Bit Line (6) for reading thereby the data reading is completed. As explained above, when the gate (G) of the transistor (T) outputs "0" data by the Logic Circuit 2 (70), transistor 3 (T3) turns "off" and then the gate (G) of the transistor (T) is floating. When "0" data is outputted from Logic Circuit 1(60), the P type (or N type) well substrate (8) is grounded. In the above process, "0" or "1" data inputted to the gate (G) can be successively read. When the source (S) of the transistor (T) reads the data, it is determined to "1" in case that measured current is more than predetermined current and to "0" in the other case. Because of comprising a pair of word line and a pair of bit line, one unit device can read the data during the other unit device writes the data. As a result, there is an improved processing speed.

Referring to FIGs. 4, 5 and 6, the fabrication method of a basic unit memory cell of the memory device comprised a single transistor is described.

FIG. 4 shows a mask pattern for fabricating the unit memory cell of the memory device comprised a single transistor.

FIG. 5 is a schematic cross sectional view showing the unit memory cell of the memory device comprised a single transistor.

FIG. 6 is a flowchart explaining a fabrication procedure of the unit memory cell of the memory device comprised the single transistor.

Referring to FIGs. 4, 5 and 6, the first step of the fabrication is forming a P type (or N type) well (8) in the N type (or P type) silicon wafer (S100).

Then, a source (S) and a drain (D) region are formed in the P type (or N type) well substrate (S200).

In order to form a gate between the source (S) and the drain (D), a gate window is opened (S300).

After opening the gate window as described in S300, a gate dielectric layer is formed in the gate region formed in S300 (S400).

And the method further comprises the steps of sputtering (or other methods) of Platinum (Pt) as a gate electrode on the gate dielectric layer (S500).

Then, a gate oxide film is formed above the gate dielectric layer (S600).

Next step is to open contact windows (30, 40 and 50 in FIG. 4) for the source (S), the drain (D), and the P type well substrate (S700).

After opening the contact windows as described in S700, metallization on each contact windows (30, 40 and 50 in FIG. 4) for the source (S), the drain (D), and the P type well substrate is done (S800).

When the metallization as described in S800 is done, the source (S) is connected to the Read Bit Line (6) (dashed line in FIG. 4), and the drain (D) is connected to the Read Word Line (5) (double-chain-dashed line in FIG. 4), and the P type (or N type) well substrate is connected to the Write Word Line (3) (solid line in FIG. 4), and the gate (G) is connected to the Write Bit Line (4) (chain-dashed line in FIG. 4) (S900).

Referring to FIG. 5, a schematic cross sectional view showing the unit memory cell of the memory device comprised a single transistor will be explained.

At first, an N type (or P type) silicon wafer having (1 0 0) direction is used. The resistivity of the silicon wafer is in the range of 2-10Ω-cm. First, form the P type(or N type) well having a 4-5μm in depth. Then, form the source(S) and the

drain(D) in the P type (or N type) well substrate. Next, after removing the oxide film of the gate(G) region, deposit a thin insulating layer, such as CeO_2, Y_2O_3, $YMNO_3$, SiO_2, SiON, etc. Then, deposit a ferroelectric thin film, such as $SrBi_2Ta_2O_9$(SBT), $PbZrTiO_3$(PZT), $PbLnZrTiO_3$(PLZT), $BaSrTiO_3$(BST), $SrBi_2TNb_2O_9$(SBTN), etc., on the thin insulator. Then, form a gate electrode using Platinum (Pt). The metallization can be done by sputtering or other methods. The electrode can be formed by Pt, Al, W, Pt/W-B-N, Pt/W-N, Al/Pt, Al/Pt/W-N, Al/Pt/W-B-N, etc. After metallization, a passivation layer is formed using Oxide and Nitride. Then, the contact windows (30, 40 and 50) in FIG. 4 for the source (S), the drain (D), and the P type well substrate is opened. After opening the contact windows, the interconnecting metallization is formed using metal, such as Al, W, Al/W, TiN/Al, etc. It is noted that the interconnecting metallization should be long enough to connect among the unit devices shown in FIG. 3. After the interconnecting metallization, the BPSG is deposited, and then planarization is done in order to planarize the device surface.

The P type(or N type) well substrate (8) itself may be the Write Word Line (3) as well as isolates each unit devices electrically. In order to isolate each unit devices electrically, instead of the P type (or N type) well substrate as described before, a buried oxide on an N type (or P type) silicon wafer or SOI (silicon on insulator) can be used. In addition, in order to isolate the P type (or N type) well substrate (8), insulating trenches are made by forming oxide layer in both sides of the P type (or N type) well substrate referring to FIG. 4. If the SOI structure is used, fabrication processes may be simpler and easier than using the P type (or N type) well because of no side diffusion process, and may accomplish large integration. When the unit memory cells are arranged in memory matrix array vertically and horizontally, it becomes a VLSI memory device, and can be used as a general memory system.

Consequently, the memory device comprising a single transistor and its fabrication method are established as intended in the present invention through the processes described above.

From the explanation up to here, the present invention provides a memory device using a single transistor, comprising a source, a drain, a ferroelectric gate formed in a P type (or N type) well substrate region. The memory device has a circuit for inputting (writing) information using a pair of writing leads which are a gate of a memory cell and a P type (or N type) well substrate and a circuit for outputting(reading) information using a pair of reading leads which are a source and a drain. And the present invention provides a fabrication method for manufacturing the

memory circuit, comprising forming the P type (or N type) well on a silicon wafer and forming the source, the drain, and then the gate on the P type (or N type) well. Since it is possible to read and write data at the same time by separating circuits for writing and reading, a very large scale integration is feasible.

The present invention is not limited to the specifically disclosed embodiments, and variations and modifications may be made without departing from the scope of the present invention.

INDUSTRIAL APPLICABILITY

With the foregoing memory device using a transistor and its fabrication in accordance with the present invention, the FRAM may have an information processing speed as fast as DRAM, as well as read/write information successively, like SRAM. Additionally, the present invention accomplishes a very large scale integration having the above advantages.

CLAIMS

1. A memory device for reading/writing data signal by using a single transistor, wherein the transistor comprises :

a first terminal, a P type(or N type) well substrate, having a P type(or N type) well which is formed on a Si wafer by diffusion or implantation of doping sources ;

a second terminal, a source ;

a third terminal, a drain ; and

a fourth terminal, a ferroelectric gate, in which the source, the drain and the gate are formed in the first terminal region.

2. A memory device as claimed in claim 1, wherein the memory device is a non-volatile, non-destructive read-out memory device which may store the written data signal successively, and read out the stored data signal without destroying the data signal.

3. A memory device as claimed in claim 1 or 2, wherein information input/output circuit comprises :

the first terminal connected to a Write Word Line (3) ;

the fourth terminal connected a Write Bit Line (4) ;

the second terminal connected a Read Word Line (5) ; and

the third terminal connected to a Read Bit Line (6).

4. A memory device as claimed in claim 1 or 2, comprising an array of a very large scale integration device by serially arraying information input/output circuit vertically and horizontally, in which the information input/output circuit comprises :

the first terminal connected to a Write Word Line (3);

the fourth terminal connected a Write Bit Line (4);

the second terminal connected a Read Word Line (5); and

the third terminal connected to a Read Bit Line (6).

5. A memory device as claimed in claim 4, wherein a data signal is inputted in the input/output circuit by designating an address through the first terminal and successively stores the data signal which is inputted through a word line of the gate(G) of the designated address.

6. A memory device as claimed in claim 4, wherein a data signal output unit of the information input/output circuit designates address for reading the data through the drain(D) of the transistor(T) and reads the data through the source(S) of the transistor(T).

7. A memory device as claimed in claim 3, wherein the information input/output circuit connected to the transistor(T), comprises :

a Logic Circuit 1 of comprising two NAND gates, in which a Word Line 1signal(10) and a write enable signal (7) are inputted into the NAND gates, and three inverters ;

a Logic Circuit 2 of comprising two NAND gates, in which a Word Line 2 signal(20) and the write enable bar signal are inputted into the NAND gates, and three inverters ;

a transistor(T1) which is connected to between output terminal of the Logic Circuit 1 and the Write Word Line (3) for writing ;

a transistor(T2) which is connected to between output terminal of the Logic Circuit 2 and the Read Bit Line (6) for reading ; and

a transistor(T3) which is connected to between another output terminal of the Logic Circuit 2 and the Write Bit Line (4) for writing, is connected to the transistor(T).

8. A memory device as claimed in claim 7, wherein when the Word Line 1signal(10) and the write enable signal(7) are inputted to the NAND gate of the Logic Circuit 1, the data signal passed inverter is inputted to the gate (G) of the transistor(T1), and then outputted to the Write Word Line (3).

9. A memory device as claimed in claim 7, wherein when the Word Line 2 signal(20) and the write enable bar signal are inputted to the NAND of the Logic Circuit 2, the data signal passed inverter is inputted to the gate (G) of the transistor 2 (T2), and then outputted to the Read Bit Line (6).

10. A memory device as claimed in claim 7, wherein when the Word Line 1 signal(10) and a write enable bar signal inverted by the inverter of the Logic Circuit 1 are inputted to the NAND gate, the data signal passed the NAND gate passes inverter and then is outputted to the Read Bit Line (6), then it is applied to the drain(D) of the

transistor(T).

11. A memory device as claimed in claim 7, wherein when Word Line 2 signal(20) and the write enable signal(7) are inputted to the NAND gate of the Logic Circuit 2, the data signal passed the NAND gate passes inverter and then is inputted to the gate(G) of the transistor(T3), then it is outputted to the Write Bit Line (4).

12. A memory device as claimed in claim 7, wherein the Write Word Line (3), Write Bit Line (4), Read Word Line (5) and Read Bit Line (6) are arranged vertically and horizontally.

13. A memory system comprising a memory device, as a memory cell, capable of writing/reading data by using a single transistor, wherein the transistor comprising :

a first terminal, a P type(or N type) well substrate which is formed on a Si wafer by diffusion or implantation of doping sources ;

a second terminal, a source ;

a third terminal, a drain ; and

a fourth terminal, a ferroelectric gate, in which the source, the drain and the gate are formed in the first terminal region.

14. A memory system as claimed in claim 13, wherein the memory device is a non-volatile, non-destructive read-out memory device which may store the written data signal successively, and read out the stored data signal without destroying the data signal.

15. A memory system as claimed in claim 13 or 14, wherein information input/output circuit comprising :

the first terminal connected to a Write Word Line (3);

the fourth terminal connected a Write Bit Line (4);

the second terminal connected a Read Word Line (5); and

the third terminal connected to a Read Bit Line (6).

16. A memory system as claimed in claim 13 or 14, comprising an array of very large scale integration device by serially arraying information input/output

circuit vertically and horizontally, in which the information input/output circuit comprising :

the first terminal connected to a Write Word Line (3);

the fourth terminal connected a Write Bit Line (4);

the second terminal connected a Read Word Line (5); and

the third terminal connected to a Read Bit Line (6).

17. A memory system as claimed in claim 13, wherein an output signal of the input/output circuit can be outputted by designating an address for reading through the drain (D) of the transistor (T), and reading the data through the source (S) of the transistor (T).

18. A memory system as claimed in claim 13, wherein an input signal of the input/output circuit can be inputted by designating an address for writing through the first terminal, and the inputted data through the Word Line of the gate (G) remains after the writing signal is removed.

19. A memory system as claimed in claim 15, wherein the information input/output circuit which is connected to the transistor(T), comprising :

a Logic Circuit 1 of comprising two NAND gates, in which a Word Line 1 signal(10) and a write enable signal(7) are inputted into the NAND gates, and three inverters ;

a Logic Circuit 2 of comprising two NAND gates, in which a Word Line 2 signal(20) and the write enable bar signal are inputted into the NAND gates, and three inverters ;

a transistor (T1) which is connected to between output terminal of the Logic Circuit 1 and the Write Word Line (3);

a transistor (T2) which is connected to between output terminal of the Logic Circuit 2 and the Read Bit Line (6); and

a transistor (T3) which is connected to between another output terminal of the Logic Circuit 2 and the Write Bit Line (4).

20. A memory system as claimed in claim 16, wherein when the Word Line 1signal(10) and the write enable signal(7) are inputted to the NAND of the Logic Circuit 1, the data signal passed inverter is inputted to the gate (G) of the first

transistor(T1), and then outputted to the Write Word Line (3).

21. A memory system as claimed in claim 16, wherein when the Word Line 2 signal(20) and the write enable bar signal are inputted to the NAND of the Logic Circuit 2, the data signal passed inverter is inputted to the gate (G) of the second transistor(T2), and then outputted to the Read Bit Line (4).

22. A memory system as claimed in claim 16, wherein when the Word Line 1signal(10) and a write enable signal(7) inverted by the inverter of the Logic Circuit 1 are inputted to the NAND gate, the data signal passed the NAND gate passes inverter and is outputted to the Read Bit Line (5), then it is applied to the drain(D) of the transistor(T).

23. A memory system as claimed in claim 16, wherein when the Word Line 2 signal(20) and the write enable signal(7) are inputted to the NAND gate of the Logic Circuit 2, the data signal passed the NAND gate passes inverter and then is inputted to the gate(G) of the transistor(T3), then it is outputted to the Write Bit Line (4).

24. A memory system as claimed in any one of claims 16 to 20, wherein the Write Word Line(3), Write Bit Line(4), Read Word Line(5), and Read Bit Line(6) are arranged vertically and horizontally.

25. A memory system as claimed in claim 21, wherein a very large scale integration device serially arrays information input/output circuit vertically and horizontally.

26. A method of fabricating a memory device, in which the memory device reads/writes data signal by using a single transistor, wherein the transistor comprises a first terminal, a P type(or N type) well substrate which is formed on a Si wafer by diffusion or implantation of doping sources, a second terminal, a source, a third terminal, a drain, and a fourth terminal, a ferroelectric gate, in which the source, the drain, and the gate are formed in the first terminal region, comprising the steps of :

forming a P type(or N type) well substrate by using a N type(P type) Si wafer ;

setting a source region and a drain region in the P type(or N type) well substrate ;

opening a gate window by isolating a gate region in order to form a gate between the source(S) and the drain(D) ;

forming a gate dielectric layer in the gate region ;

depositing a Pt, as a gate electrode, on the gate dielectric layer ;

forming a gate oxide film above the gate dielectric layer ;

opening a contact window of opening each contact window of the source(S), the drain(D), and the P type(or N type) well substrate ;

depositing a contact window metal on each contact window ; and

connecting the source(S) to a Read Bit Line, the drain(D) to a Read Word Line, the P type(or N type) well substrate to a Write Word Line, and the gate(G) to a Write Bit Line.

27. A method of fabricating a memory device as claimed in claim 26, wherein the memory device is a non-volatile, non-destructive read-out memory device which may store the written data signal successively, and read out the stored data signal without destroying the data signal.

28. A method of fabricating a memory device as claimed in claim 26 or 27, wherein the P type(or N type) well substrate is used for the P type(or N type) well substrate terminal in case of using a N type(or P type) Si-wafer.

29. A method of fabricating a memory device as claimed in claim 28, wherein the P type(or N type) well substrate is used by isolating from a memory cell of the memory device.

30. A method of fabricating a memory device as claimed in claim 28, wherein an electrode used in the gate electrode depositing step, uses a Pt.

31. A method of fabricating a memory device as claimed in claim 28, wherein an electrode used in the gate electrode depositing step, uses an Al.

32. A method of fabricating a memory device as claimed in claim 28, wherein an electrode used in the gate electrode depositing step, uses a W.

33. A method of fabricating a memory device as claimed in claim 28, wherein an electrode used in the gate electrode depositing step, uses a Pt/W-B-N.

34. A method of fabricating a memory device as claimed in claim 28, wherein an electrode used in the gate electrode depositing step, uses a Pt/W-N.

35. A method of fabricating a memory device as claimed in claim 28, wherein an electrode used in the gate electrode depositing step, uses an Al/Pt.

36 A method of fabricating a memory device as claimed in claim 28, wherein an electrode used in the gate electrode depositing step, uses an Al/Pt/ W-N.

37. A method of fabricating a memory device as claimed in claim 28, wherein an electrode used in the gate electrode depositing step, uses an Al/Pt/W-B-N.

38. A method of fabricating a memory device as claimed in claim 28, wherein a ferroelectric layer used in the gate dielectric layer forming step, is a ferroelectric film of SBT($SrBi_2Ta_2O_9$).

39. A method of fabricating a memory device as claimed in claim 28, wherein a ferroelectric layer used in the gate dielectric layer forming step, is a ferroelectric film of PZT($PbZrTiO_3$).

40. A method of fabricating a memory device as claimed in claim 28, wherein a ferroelectric layer used in the gate dielectric layer forming step, is a ferroelectric film of PLZT($PbLnZrTiO_3$).

41. A method of fabricating a memory device as claimed in claim 28, wherein a ferroelectric layer used in the gate dielectric layer forming step, is a ferroelectric film of BST($BaSrTiO_3$).

42. A method of fabricating a memory device as claimed in claim 28, wherein a ferroelectric layer used in the gate dielectric layer forming step, is a ferroelectric film of SBTN($SrBi_2TNb_2O_9$).

43. A method of fabricating a memory device as claimed in claim 28, wherein an insulating layer used in the gate dielectric layer forming step, uses CeO_2.

44. A method of fabricating a memory device as claimed in claim 28, wherein an insulating layer used in the gate dielectric layer forming step, uses Y_2O_3.

45. A method of fabricating a memory device as claimed in claim 28, wherein an insulating layer used in the gate dielectric layer forming step, uses $YMNO_3$.

46. A method of fabricating a memory device as claimed in claim 28, wherein an insulating layer used in the gate dielectric layer forming step, uses SiO_2.

47. A method of fabricating a memory device as claimed in claim 28, wherein an insulating layer used in the gate dielectric layer forming step, uses SiON.

48. A method of fabricating a memory device as claimed in any one of claims 26 to 47, wherein a lower Si wafer uses an SOI(silicon on insulator) which is formed on the insulating layer.

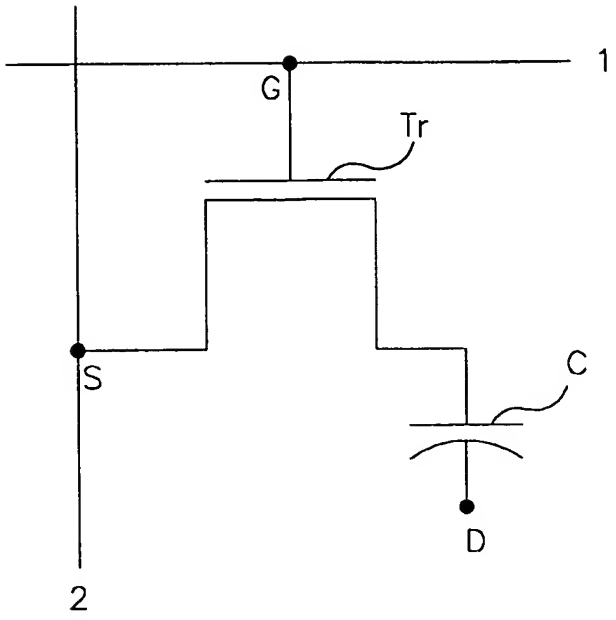

FIG. 1

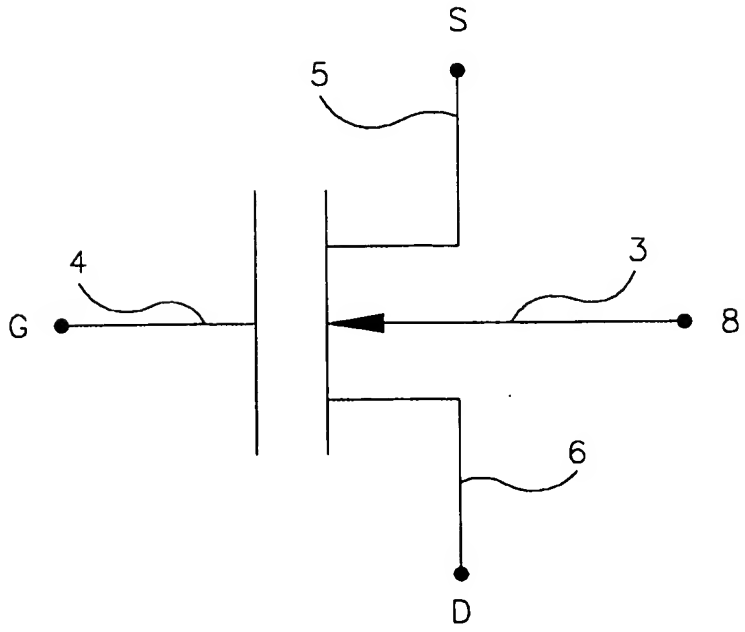

FIG. 2

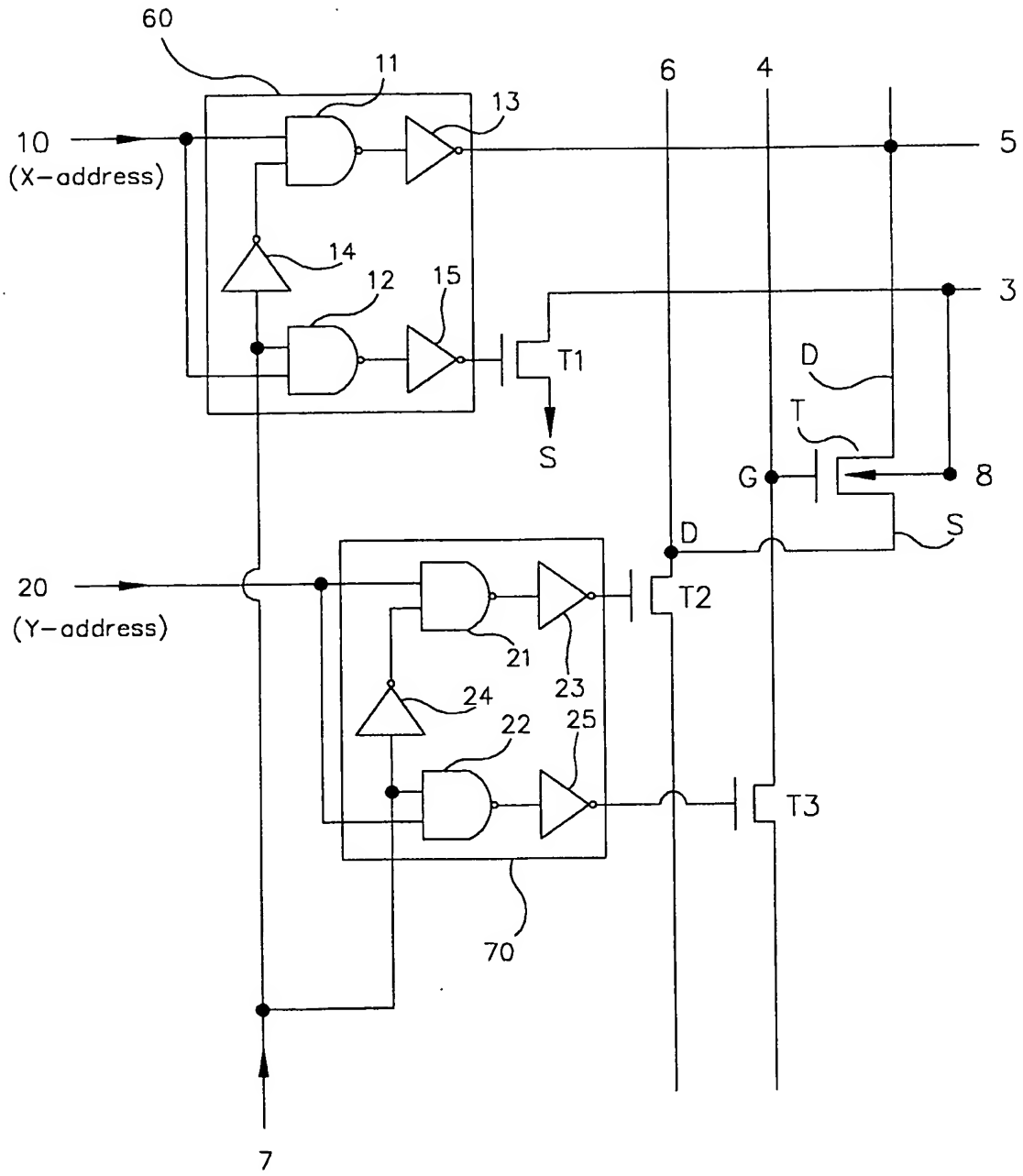
60
11
13
6
4
10
(X-address)
5
14
12
15
3
T1
S
D
T
G
8
S
D
20
(Y-address)
T2
21
23
24
22
25
T3
70
7

FIG. 3

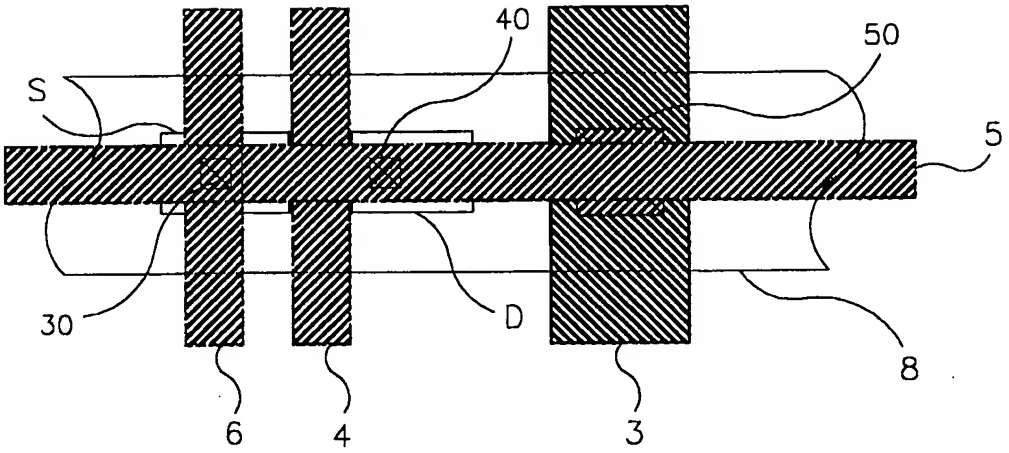
40
50
S
5
30
D
8
6
4
3

FIG. 4

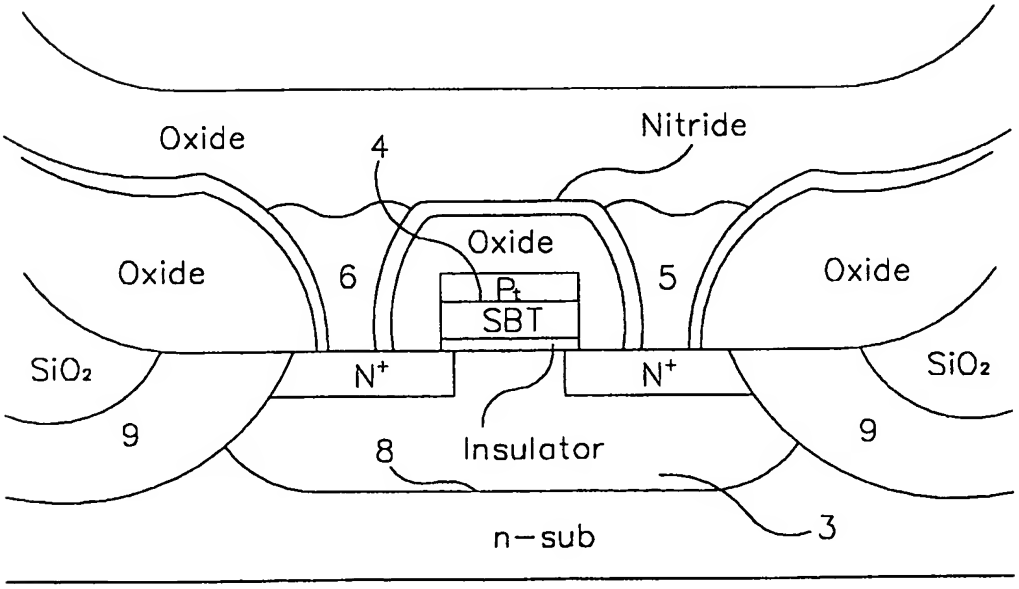
Oxide
4
Nitride
Oxide
Oxide
6
Pt
SBT
5
Oxide
SiO2
N+
N+
SiO2
9
8
Insulator
9
3
n-sub

FIG. 5

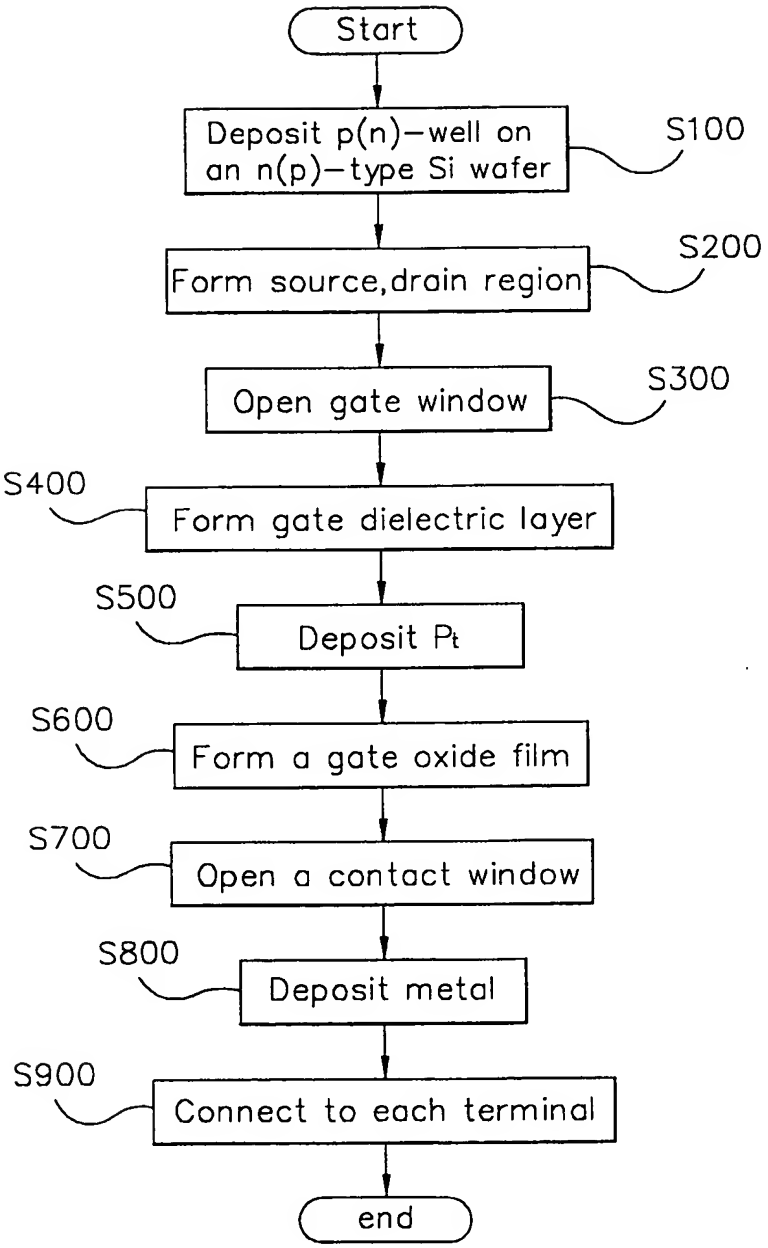
Start
Deposit p(n)-well on an n(p)-type Si wafer
S100
Form source,drain region
S200
Open gate window
S300
S400
Form gate dielectric layer
S500
Deposit Pt
S600
Form a gate oxide film
S700
Open a contact window
S800
Deposit metal
S900
Connect to each terminal
end

FIG. 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR 99/00086

A. CLASSIFICATION OF SUBJECT MATTER

IPC[6]: G 11 C 7/00, 11/40

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC[6]: G 11 C 7/00, 11/34, 11/36, 11/40, 11/44

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 388 068 A (GHOSHAL et al.) 07 February 1995 (07.02.95).	1,13,26
A	US 5 671 181 A (HATSUDA) 23 September 1997 (23.09.97).	1,13,26
A	US 5 587 944 A (SHEN et al.) 24 December 1996 (24.12.96).	1

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
„A" document defining the general state of the art which is not considered to be of particular relevance
„E" earlier application or patent but published on or after the international filing date
„L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
„O" document referring to an oral disclosure, use, exhibition or other means
„P" document published prior to the international filing date but later than the priority date claimed
„T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
„X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
„Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
„&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
04 May 1999 (04.05.99)	21 June 1999 (21.06.99)

Name and mailing adress of the ISA/AT	Authorized officer
Austrian Patent Office Kohlmarkt 8-10; A-1014 Vienna Facsimile No. 1/53424/200	Grössing Telephone No. 1/53424/386

Form PCT/ISA/210 (second sheet) (July 1998)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR 99/00086

All documents retrieved exhibit a memory device using a transistor, read and write terminals and means for inputting and outputting of information.

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/KR 99/00086

In Recherchenbericht angeführtes Patentdokument Patent document cited in search report Document de brevet cité dans le rapport de recherche	Datum der Veröffentlichung Publication date Date de publication	Mitglied(er) der Patentfamilie Patent family member(s) Membre(s) de la famille de brevets	Datum der Veröffentlichung Publication date Date de publication
US A 5388068	07-02-1995	JP T2 5507587 US A 5024993 WO A1 9117569	28-10-1993 18-06-1991 14-11-1991
US A 5671181	23-09-1997	JP A2 8235870 JP B2 2869369	13-09-1996 10-03-1999
US A 5587944	24-12-1996	keine - none - rien	